ABSTRACT

A delay addressed data path register file is designed for use in a programmable processor making up a cell in a multi-processor or array signal processing system. The delay addressable register file is particularly useful in, ***inter alia***, adaptive filters where the filter update latency is variable, interpolation filters where the interpolation factor needs to be programmable, and decimation filters where the decimation factor needs to be programmable. The programmability is achieved in an efficient manner, reducing the number of cycles required to perform this task. A single parameter, the "delay limit" value, is programmed at start-up, setting up an internal delay-line within the register file of the processor. Thus, any of the delayed registers can be addressed by specifying the delay index during run-time. The delay line advances one location, modulo "delay-limit", when the processing loop starts a new iteration.